

Project Name : A14IM01\_DDR3

Platform : Montevina Penryn(CPU)+Cantiga(NB)+ICH9M(SB)

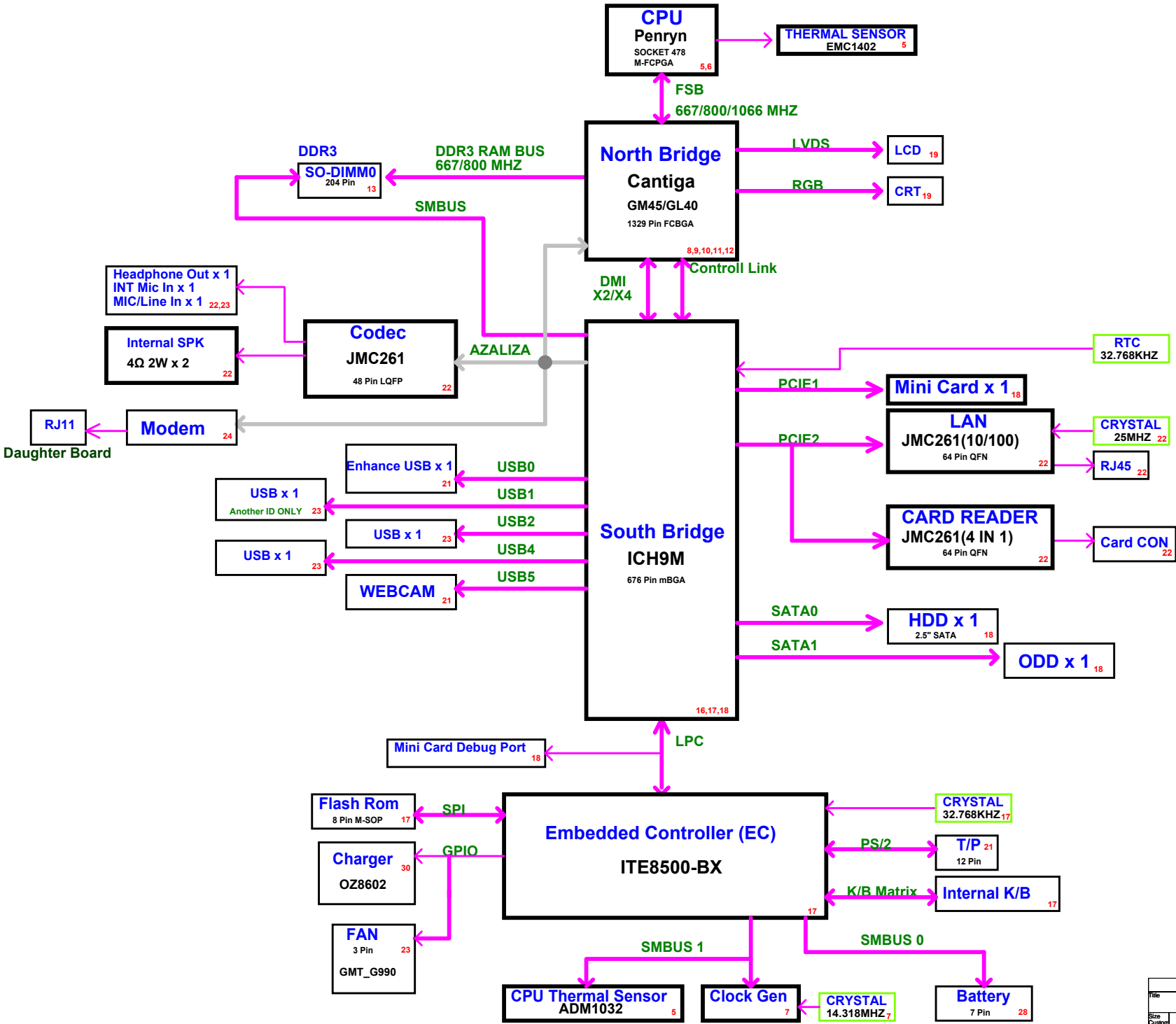
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M/B Schematic Version Change List

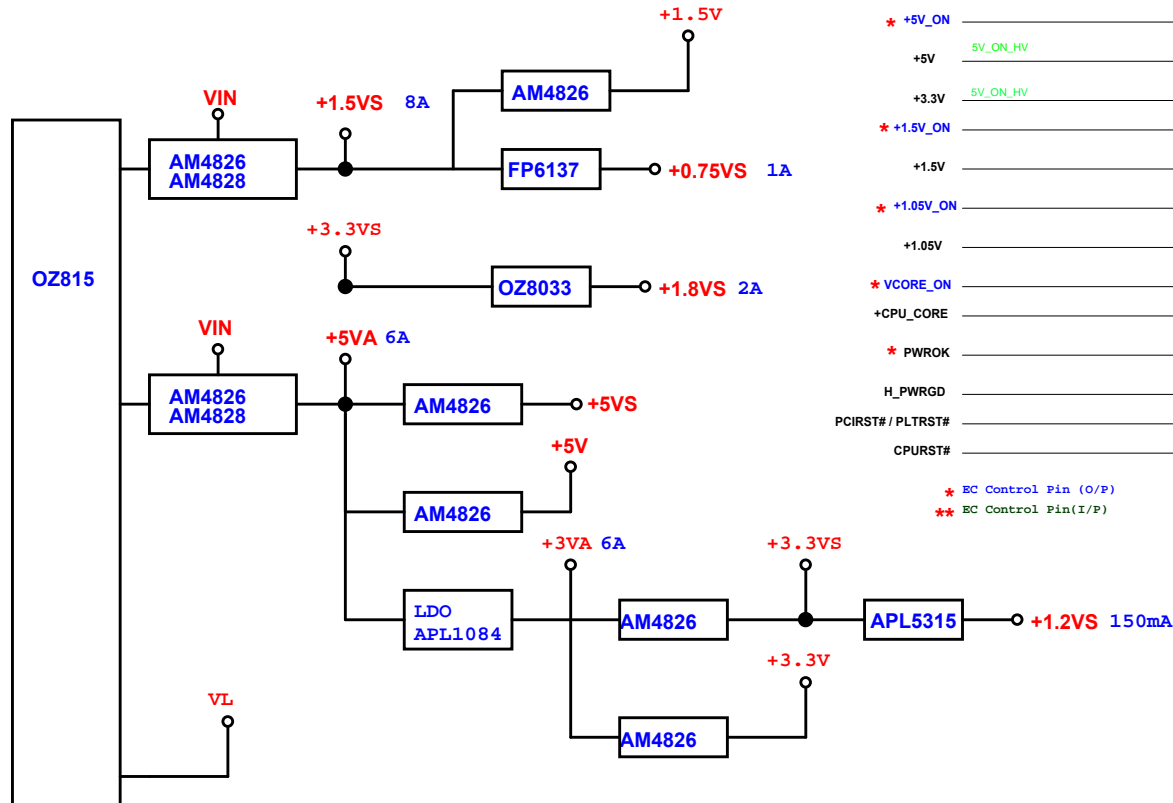
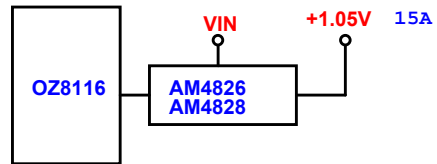
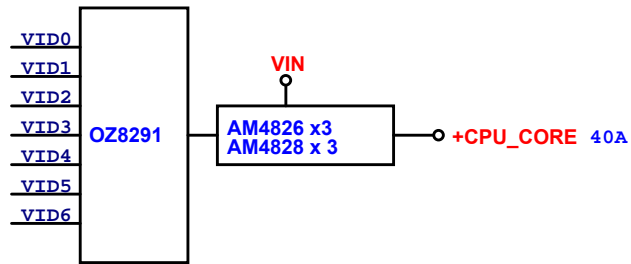
Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

A14IMXX M/B V1.0 DDR3 (01 SLOT DDR3)  
71R-R14IM0-T810  
Esquemático REV A  
Na página 30 lista com as modificações REV B  
A14IMXX A14IM01

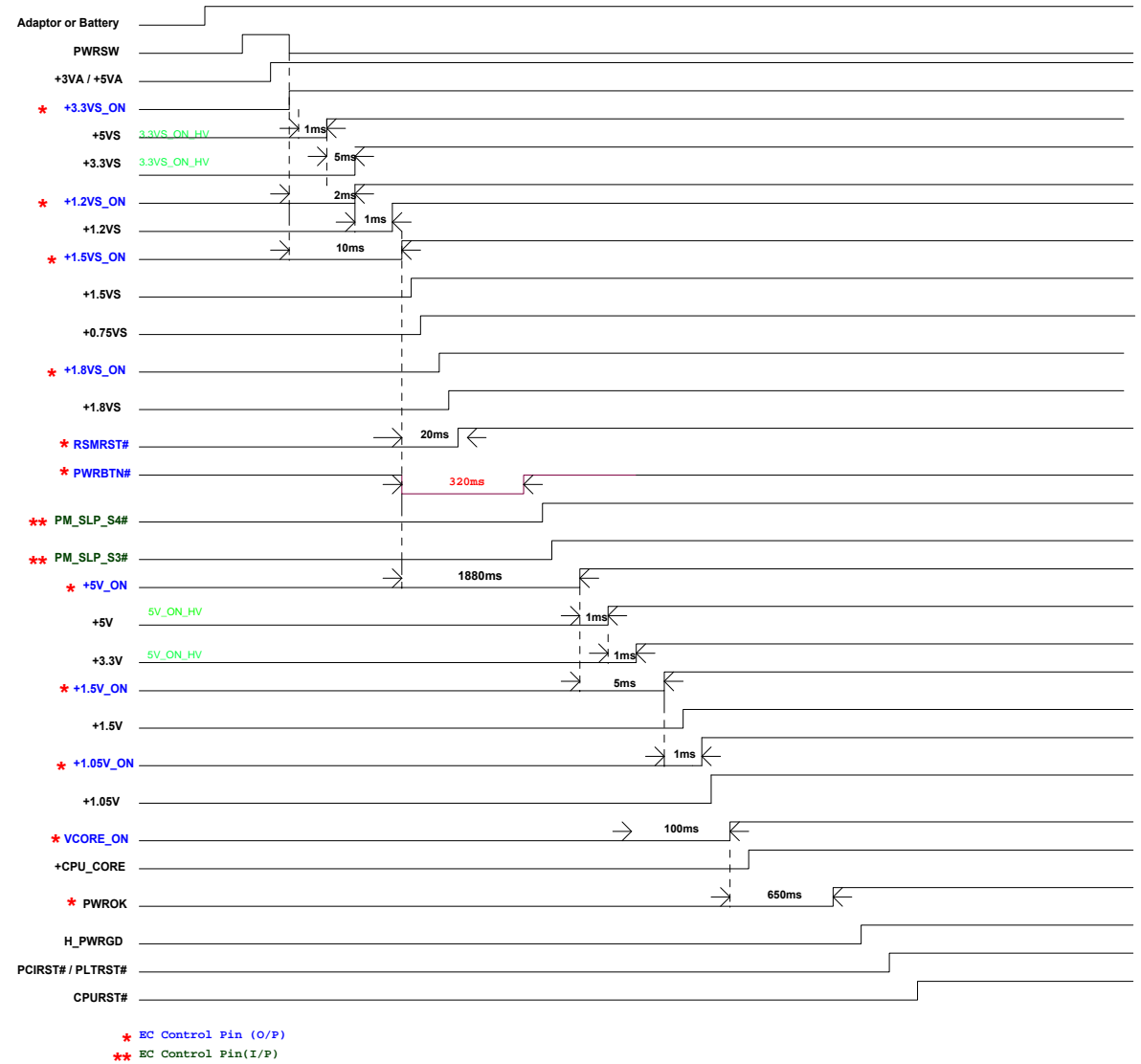
SYSTEM BLOCK DIAGRAM



# POWER BLOCK DIAGRAM



# System Poewr On Sequence



ICH9M GPIO	
GPIO0	PM_BM_BUSY#
GPIO1	EC_EXTSMI#
GPIO2	INT_PIRQE#
GPIO3	INT_PIRQF#
GPIO4	INT_PIRQG#
GPIO5	INT_PIRQH#
GPIO6	BIOS_REC
GPIO7	<b>N.C</b> (TACH3)
GPIO8	<b>N.C</b>
GPIO9	<b>N.C</b> (WOL_EN)
GPIO10	<b>N.C</b> (ALERT#)
GPIO11	SMB_ALERT#
GPIO12	LAN_PHYPC
GPIO13	<b>N.C</b> (GLAN_DOCK#)
GPIO14	<b>N.C</b> (NETDETECT)
GPIO15	PM_STPPCI#
GPIO17	<b>N.C</b> (TACH0)
GPIO18	<b>N.C</b>
GPIO19	SATA1GP
GPIO21	SATA0GP
GPIO22	<b>N.C</b> (SCLOCK)
GPIO23	LDRQ1#
GPIO24	CRB_SV_DET
GPIO25	PM_STPCPU#
GPIO26	PM_SLP_S4_STATE#
GPIO27	QRT_STATE0
GPIO28	QRT_STATE1
GPIO29	USB_OC#5
GPIO30	USB_OC#6
GPIO31	USB_OC#7
GPIO32	PM_CLKRUN#
GPIO33	HDA_DOCK_EN
GPIO34	<b>N.C</b> (HDA_DOCK_RST)
GPIO35	CLK_SATA_OE#
GPIO36	SATA2GP
GPIO37	SATA3GP
GPIO38	ODD_DET
GPIO39	ICH_GPIO39
GPIO40	USB_OC#1
GPIO41	USB_OC#2
GPIO42	USB_OC#3
GPIO43	USB_OC#4
GPIO48	MFG_MODE
GPIO49	H_PWRGD
GPIO50	PCI_REQ#1
GPIO51	PCI_GNT#1
GPIO52	PCI_REQ#2
GPIO53	PCI_GNT#2
GPIO54	PCI_REQ#3
GPIO55	PCI_GNT#3

ITE8510 GPIO		Default Pull/Mode
GPA0	RF_LED#	UP / GPI
GPA1	EC_BSEL1	UP / GPI
GPA2	BT_L_BEEP	UP / GPI
GPA3	WLAN_PWR#	UP / GPI
GPA4	P_ID0	UP / GPI
GPA5	P_ID1	UP / GPI
GPA6	PM_RSMRST#	UP / GPI
GPA7	EC_BL_PWM	UP / GPI
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	+1.05V_ON	Dn / GPI
GPB3	BAT_SMBCLK	/ GPI
GPB4	BAT_SMBDAT	/ GPI
GPB5	H_A20GATE	/ GPO
GPB6	H_RCIN#	UP / Funcl
GPB7	ENHANCE_USB#	Dn / GPI
GPC0	+1.5V_ON	Dn / GPI
GPC1	SMB_CLK_EC	/ GPI
GPC2	SMB_DAT_EC	/ GPI
GPC3	<b>N.C</b>	Dn / GPI
GPC4	SAVE_POWER	Dn / GPI
GPC5	SLP_S4_COY	Dn / GPI
GPC6	+3.3VS_ON	Dn / GPI
GPC7	CRT_DETECT	UP / GPI
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPI
GPD2	PLT_RST#	UP / Funcl
GPD3	<b>N.C</b>	UP / GPI
GPD4		UP / GPI
GPD5	PWR_USB_LED#	UP / GPI
GPD6	<b>N.C</b>	Dn / GPI
GPD7	SET_V	Dn / GPI
GPE0	LID#	Dn / GPI
GPE1	Fastcharge_EN	Dn / GPI
GPE2	PWROK	Dn / GPI
GPE3	Vcore_ON	Dn / GPI
GPE4	PWRSW	UP / GPI
GPE5	+1.2VS_ON	Dn / GPI
GPE6	WLAN_ON	Dn / GPI
GPE7	AMP_MUTE#	UP / GPI
GPF0	<b>N.C</b>	UP / GPI
GPF1	<b>N.C</b>	UP / GPI
GPF2	<b>N.C</b>	UP / GPI
GPF3	CHG_ON#	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	<b>N.C</b>	UP / GPI
GPF7	<b>N.C</b>	UP / GPI
GPG0	+3.3VA	Dn/GPO/TM
GPG1	+5V_ON	Dn/GPO/ID7
GPG2	<b>N.C</b>	
GPG6	WEBCAN_ON	Dn / GPI
GPH0	SAFETY_PROTECT	Dn/GPI/ID0
GPH1	+1.8VS_ON	Dn/GPI/ID1
GPH2	SENBAT_V	Dn/GPI/ID2
GPH3	CHG_G_LED	Dn/GPI/ID3
GPH4	CHG_R_LED	Dn/GPI/ID4
GPH5	BATOFF	Dn/GPI/ID5
GPH6	PWR_LED	Dn/GPI/ID6

ITE8510 GPIO		Default Pull/Mode
GPI0	<b>N.C</b>	/GPI/ADC
GPI1	LCDSW0	/GPI/ADC
GPI2	LCDSW1	/GPI/ADC
GPI3	<b>N.C</b>	/GPI/ADC
GPI4	BAT_I	/GPI/ADC
GPI5	BATT_TEMP	/GPI/ADC
GPI6	ADAPTOR_1	/GPI/ADC
GPI7	BAT_V	/GPI/ADC
GPJ0	EC_BL_ON	/GPI/DAC
GPJ1	EC_PROCHOT	/GPI/DAC
GPJ2	FAN_CTRL0	/GPI/DAC
GPJ3	CHG_REF	/GPI/DAC
GPJ4	CHG_I	/GPI/DAC
GPJ5	PM_THROTTLING#	/GPI/DAC

Penryn CPU				
	CPU CORE(V)	ICC(A)	W	TEMP(℃)
IMVP-6+	1.05	44.0	36	

Cantiga			
VCC	ICC(mA)	W	TEMP(℃)
+3.3V	262	0.87	105
+1.8VS	3249	5.73	
+1.5V	86	0.129	
+1.05	14688.52	15.43	

ICH9M			
VCC	ICC(mA)	mW	TEMP(℃)
+5V	4	20	70
+5VS	2	10	
+3.3V	347	1145.1	
+3.3VS	212	699.6	
+1.5V	1988	2982	
+1.05V	1634	1715.7	

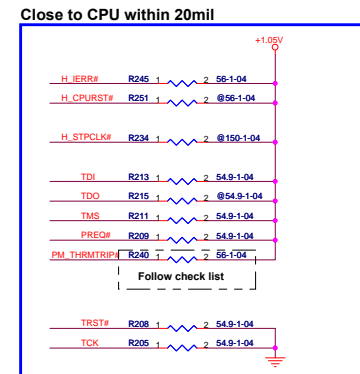
ITE8500			
VCC	ICC(mA)	mW	TEMP(℃)
+3.3V	100	330	70

CLOCK GENERATOR			
VCC	ICC(mA)	mW	TEMP(℃)
+3.3V	1000	3300	70

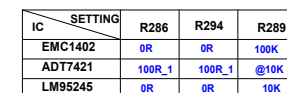
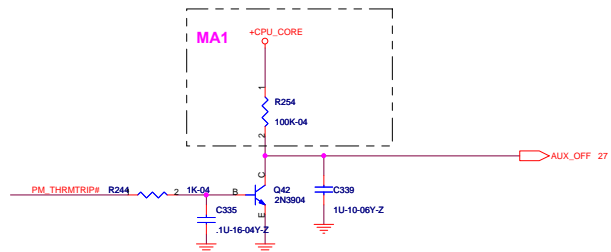
IDT92HD81			
VCC	ICC(mA)	mW	TEMP(℃)
+3.3V(DVDD)	200	660	70
+5V(AVDD)	1000	5000	

ADM1032			
VCC	ICC	mW	TEMP(℃)
+3.3V	170uA	0.56	150

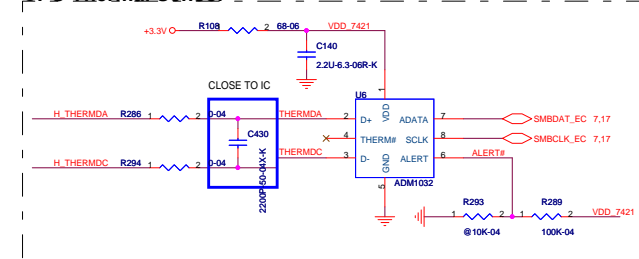
JMC261			
VCC	ICC(mA)	mW	TEMP(℃)
+3.3VS	300	990	70
+1.2VS	150	180	



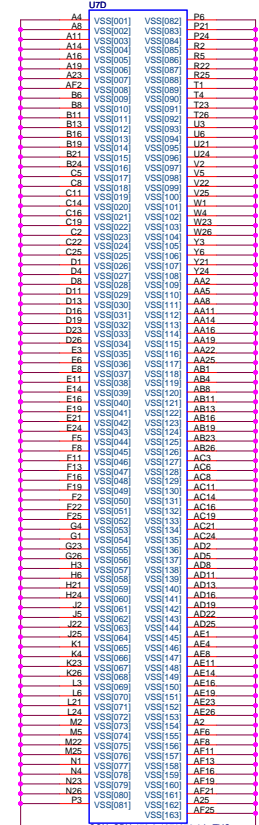
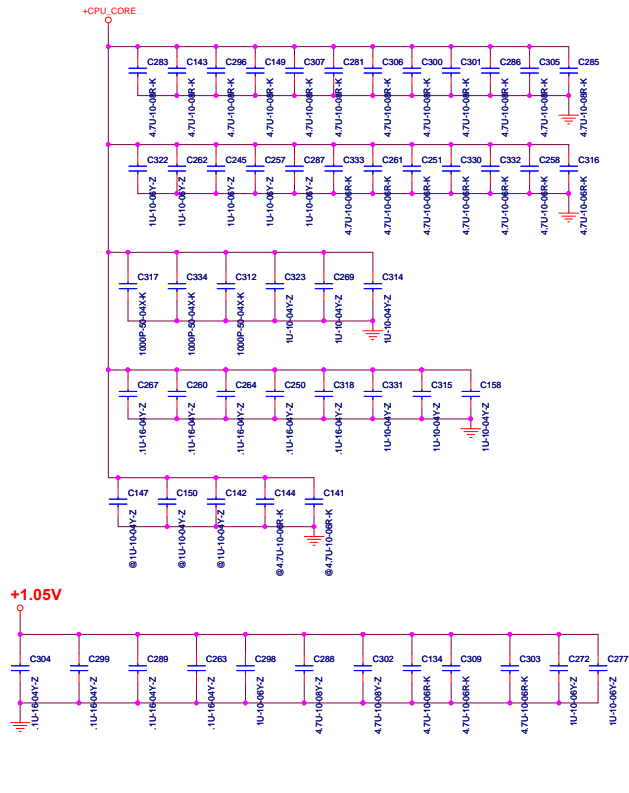
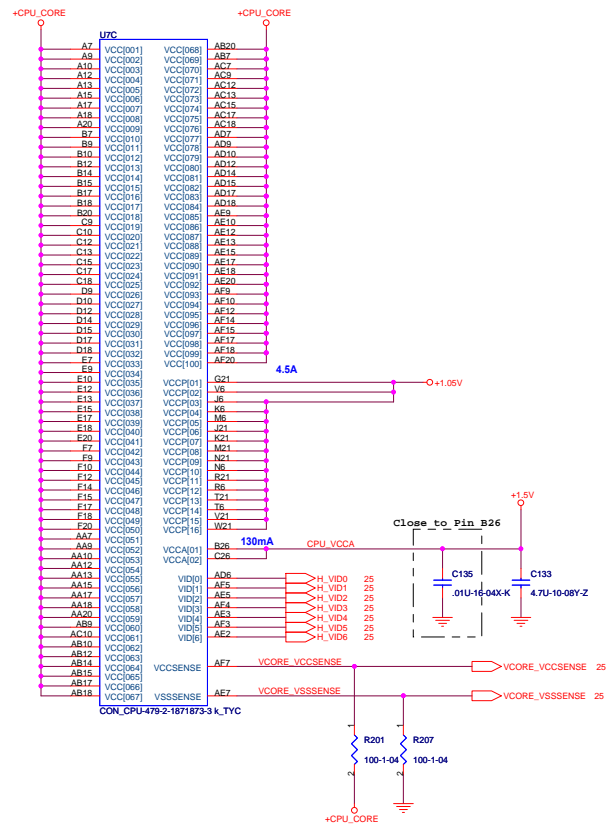
FSB \ BSEL	BSEL2	BSEL1	BSEL0	MHZ
FSB667	0	1	1	166
FSB800	0	1	0	200
FSB1066	0	0	0	266

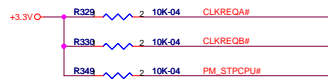


R289 can use 100K for 3 vender real application  
R286,R294 can use 0-04 for ADT7421 real application

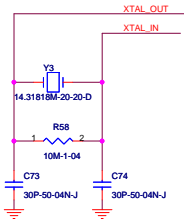
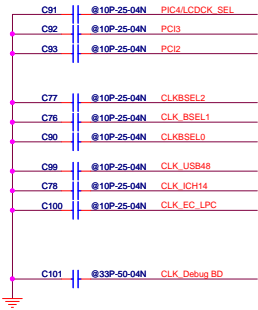


### For OverClock CPU SIDE

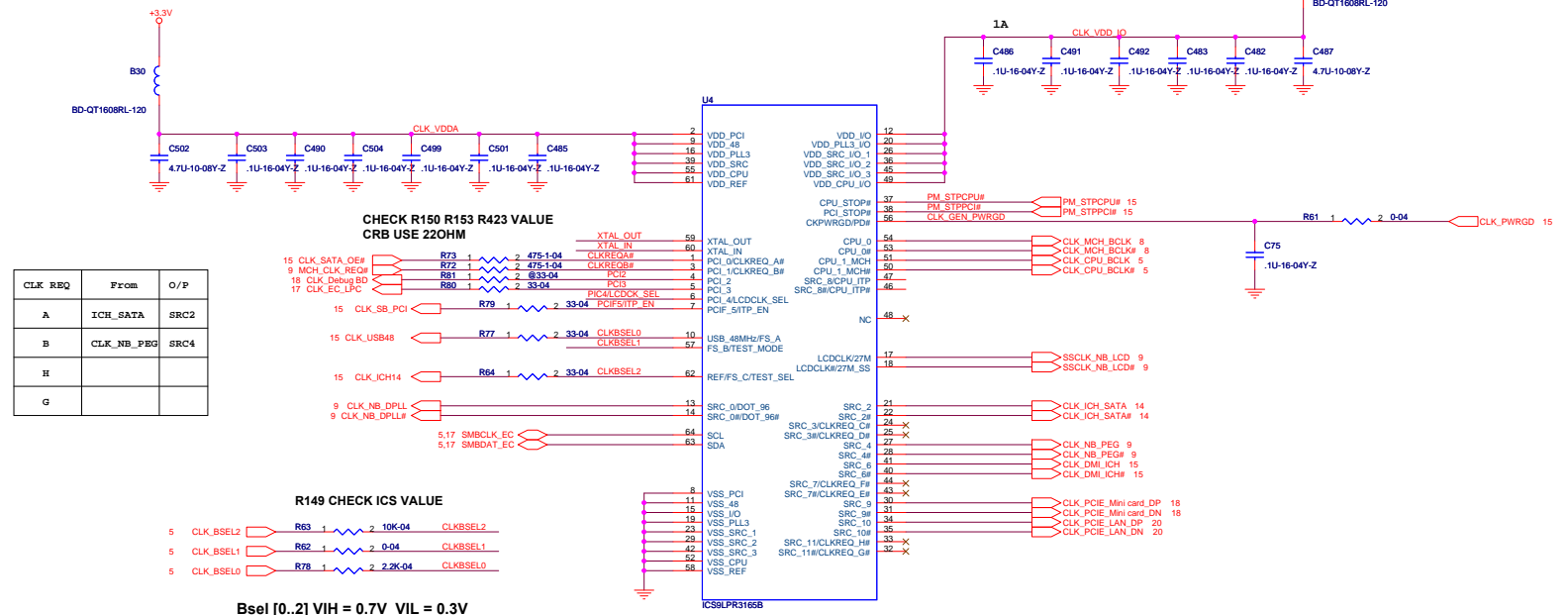




Reserved FOR EMI

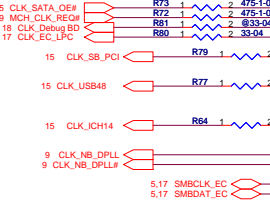


$C_e = 2 * CL - (C_s + C_i)$   
 CL = Crystal Load Cap = 20P  
 C<sub>i</sub> = IC internal Cap = 5P  
 C<sub>s</sub> = 2P  
 C<sub>e</sub> = Crystal external Cap = 33P



CLK REQ	From	O/P
A	ICH_SATA	SRC2
B	CLK_NB_PEG	SRC4
H		
G		

CHECK R150 R153 R423 VALUE  
CRB USE 220HM



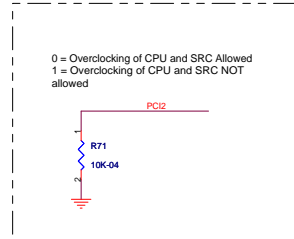
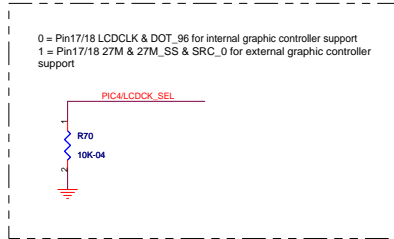
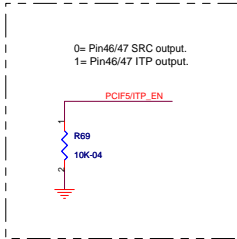
R149 CHECK ICS VALUE

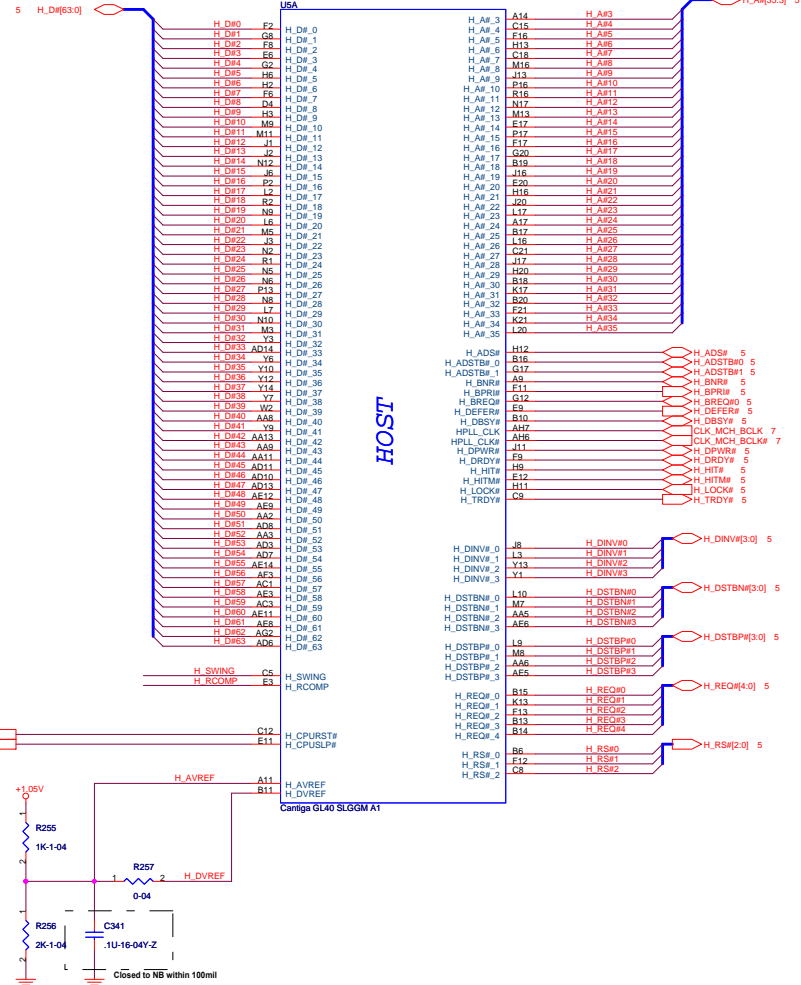
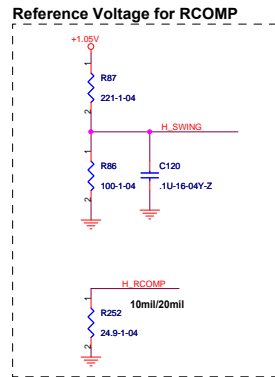
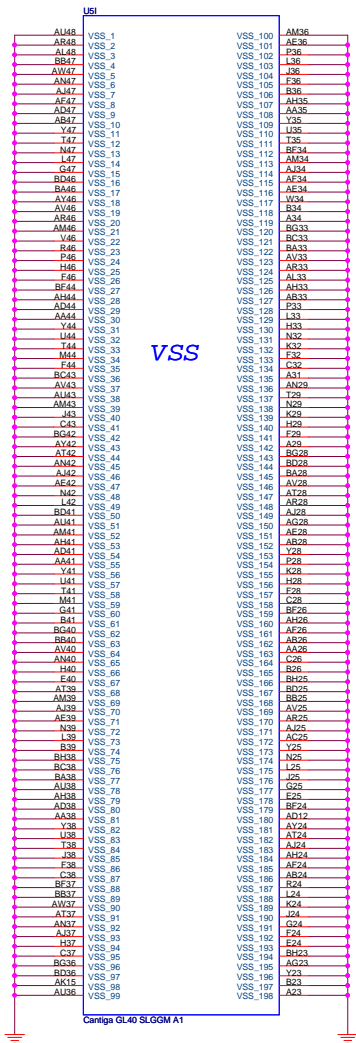


Bsel [0..2] VIH = 0.7V VIL = 0.3V

FSB	BSEL	BSEL2 FSLC	BSEL1 FSLB	BSEL0 FSLA	CPU MHZ	PCI MHZ	PCI-E MHZ
FSB667	0	1	1	166			
FSB800	0	1	0	200	33	100	
FSB1066	0	0	0	266			

\*Need reserved space for 72Pin CLOCK GEN\*

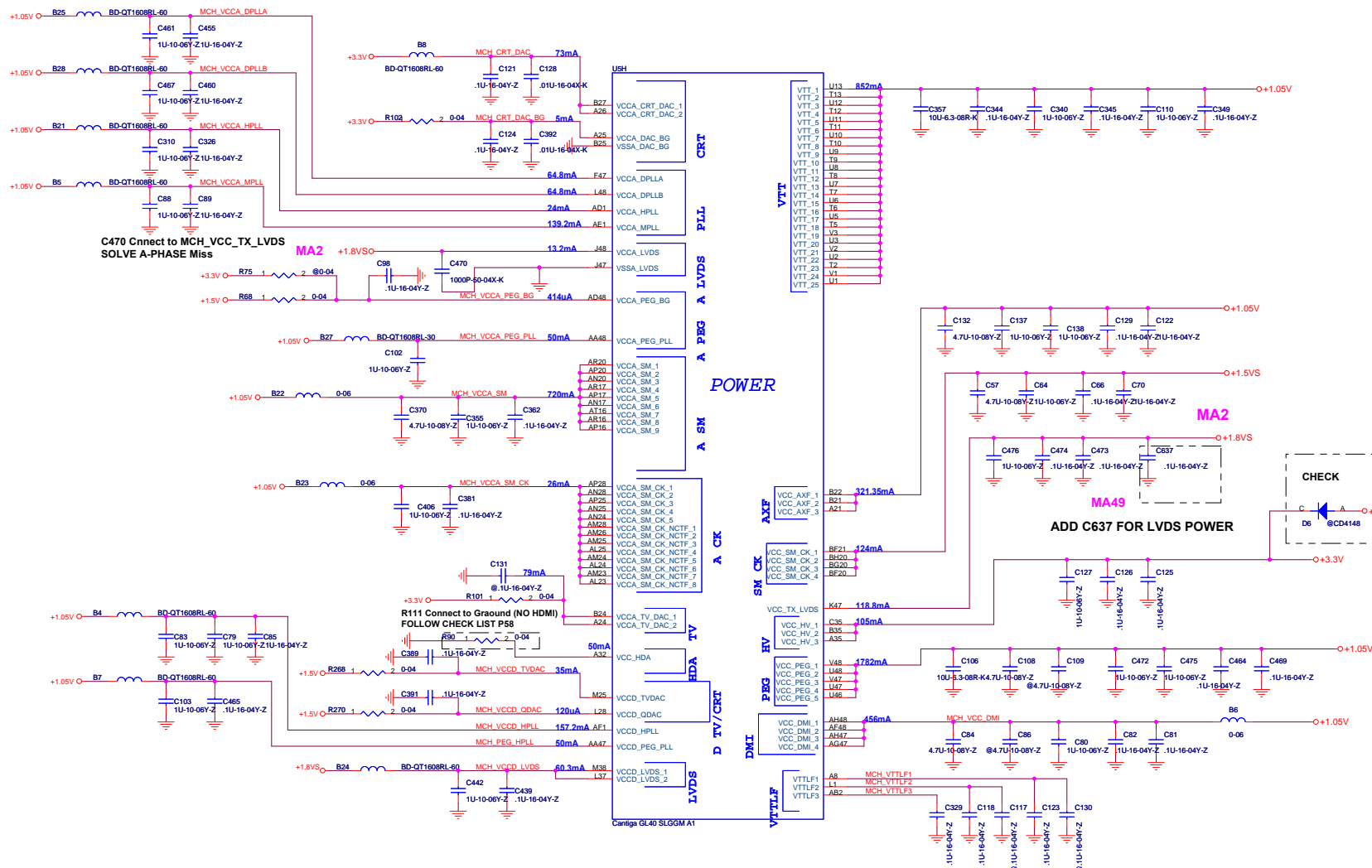


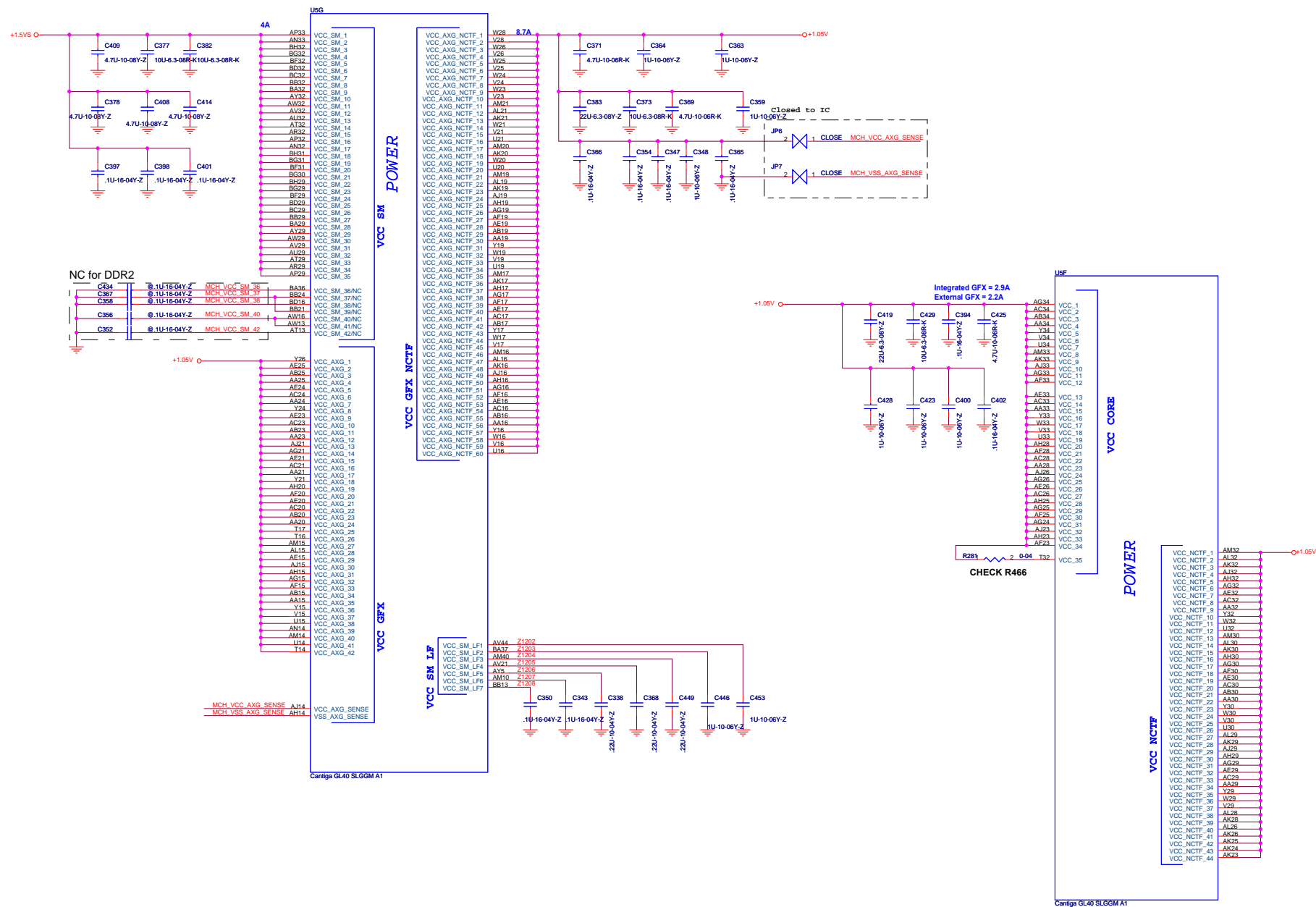




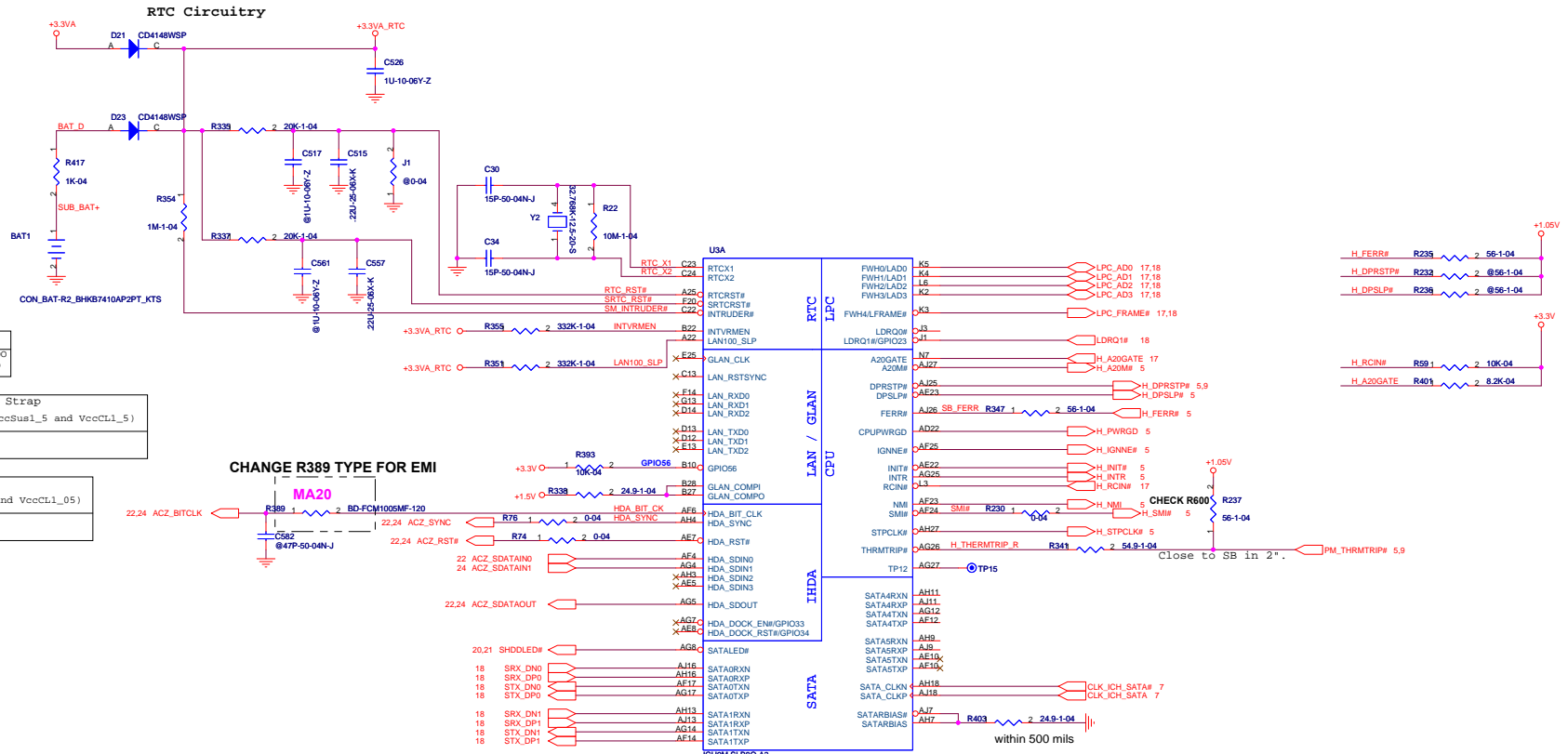












SM\_INTRUDER#  
0 = Disable Internal 1.5Vs LDO  
1 = Enable Internal 1.5Vs LDO

ICH9-M Internal VR Enable Strap  
(Internal VR for VccSusi\_05, VccSusi\_5 and VccCL1\_5)  
Low = Internal VR Disabled  
High = Internal VR Enabled  
(Default)

ICH9-M LAN100\_SLP Strap  
(Internal VR for VccLAN1\_05 and VccCL1\_05)  
Low = Internal VR Disabled  
High = Internal VR Enabled  
(Default)









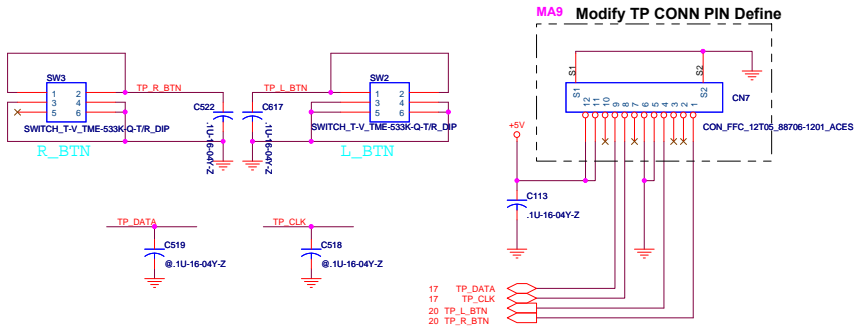




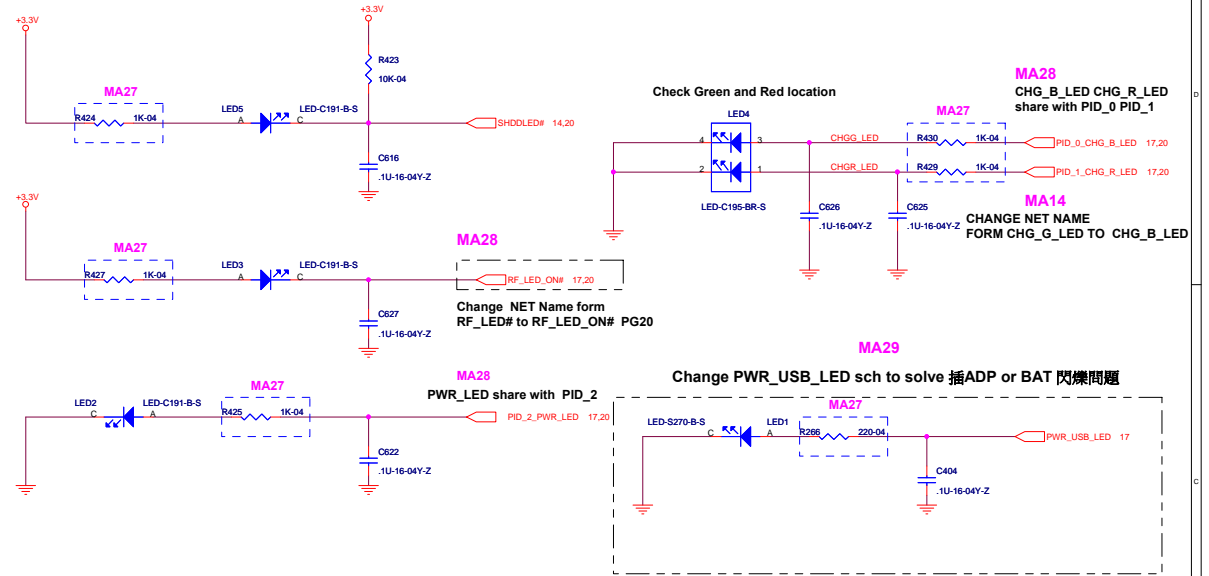




## Touch Pad

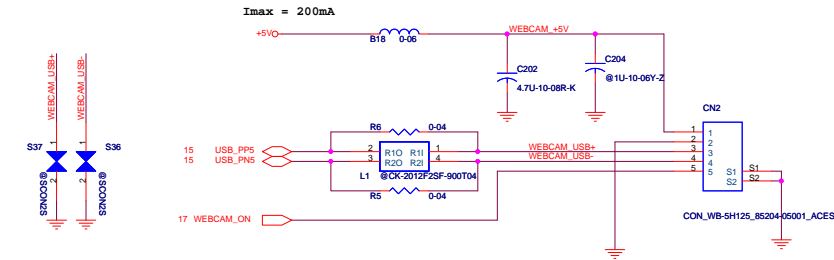


## LED MA27 - R424,R427,R425,R430,R429,R266 Change to 220-04

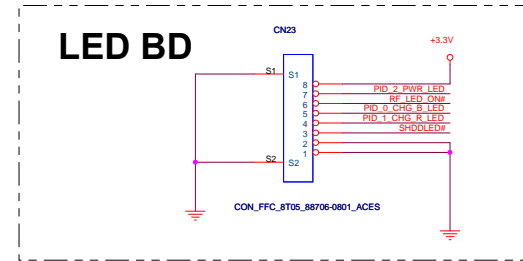


## WEBCAM CON

WEBCAM_ON	
1	ON
0	OFF



## LED BD



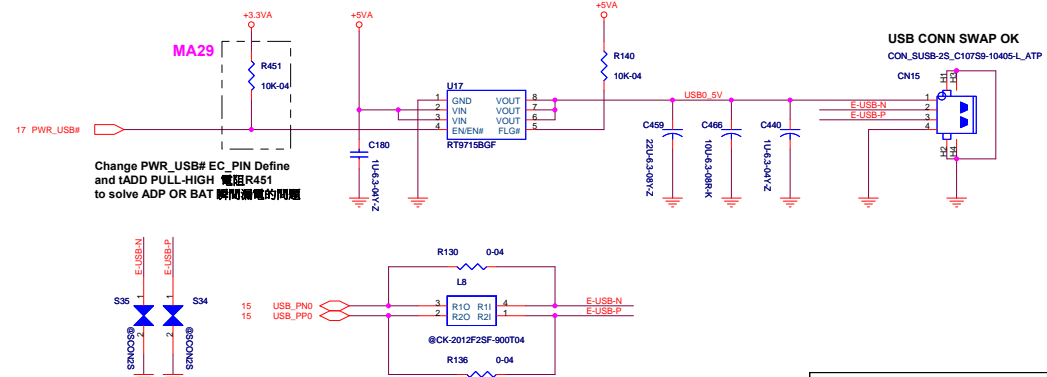
MA14 ADD LED CONN CN23

MA28 Change CN23 PIN7 NET Name form RF\_LED# to RF\_LED\_ON# PG20

CHG\_B\_LED CHG\_R\_LED PWR\_LED share with PID\_0 PID\_1 PID\_2

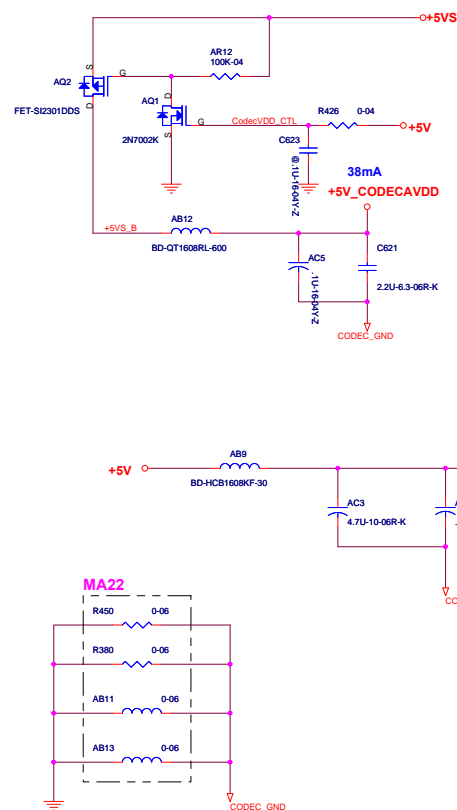
MA14 CHANGE CN23 PIN5 DEFINE FORM CHG\_G\_LED TO CHG\_B\_LED

## ENHANCE USB Port

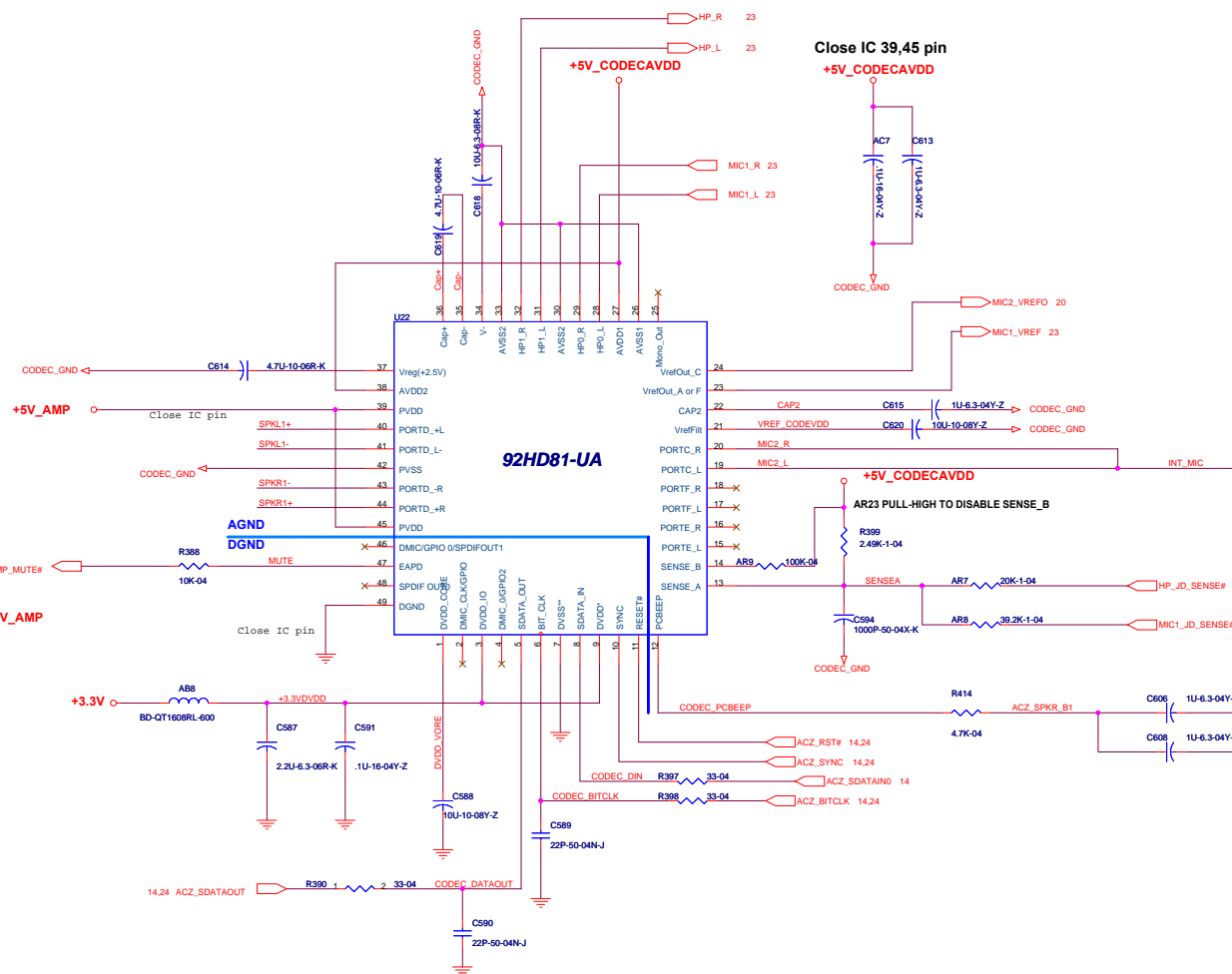


**CODEC 92HD81**

**AMP VDD**



**CHANGE R450,R380,AB11,AB13 to 0ohm for EMI**

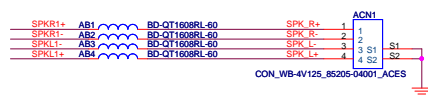
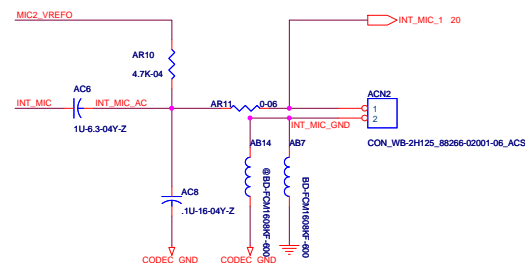


**SENSE\_A Channel**

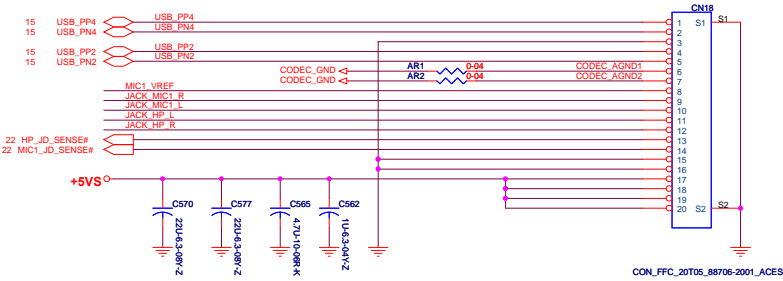
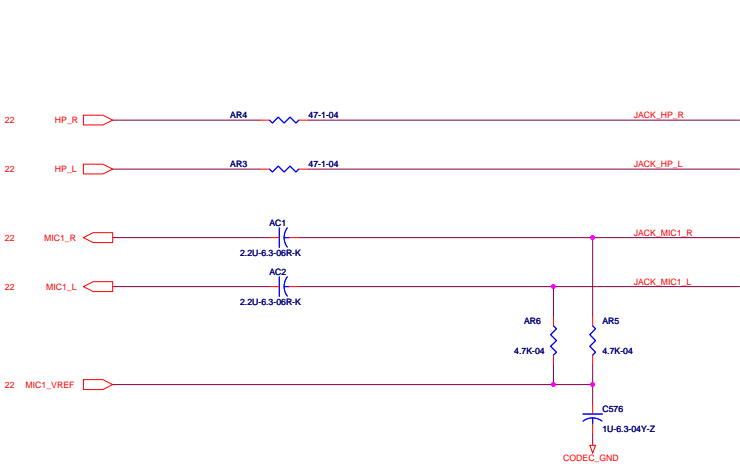
HP0-MIC-IN LINE-IN  
HP1-HEADPHONE-OUT LINE-OUT

39.2K PORTA HP0  
20K PORTB HP1

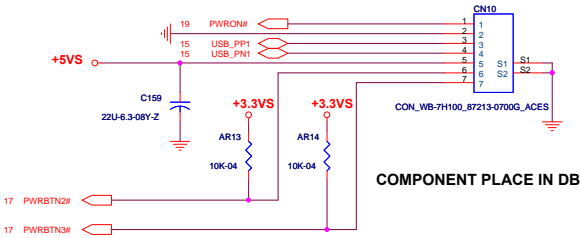
## INT\_SPEAKER

**INT\_MIC**

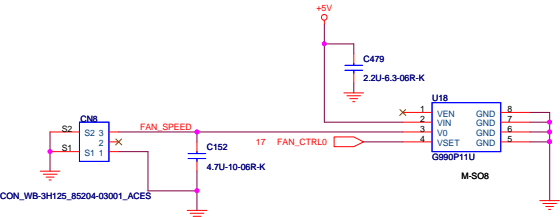
# EXT MIC/EXT Line In/ EXT USB JACK



## EXT USB PORT 4



## CPU FAN CONTROL







VID: 0.8~1.175V  
Icc max: 40A  
LLS: set to 2.1mV/A

ADD R432 Pull-High to +3.3V in DELAY\_VR\_PWRGOOD solve open issue

B16 上件 , JP2 OPEN FOR EMI

CHECK BATTERY Leacking current

MA45 ADD C641 C642 FOR EMI

OCP:50A

MA45 Change C201 to 0402 type

DEL-CSN-Connect-to-GND NET

MA45 ADD JP9 FOR EMI

Change C215 Location BY O2

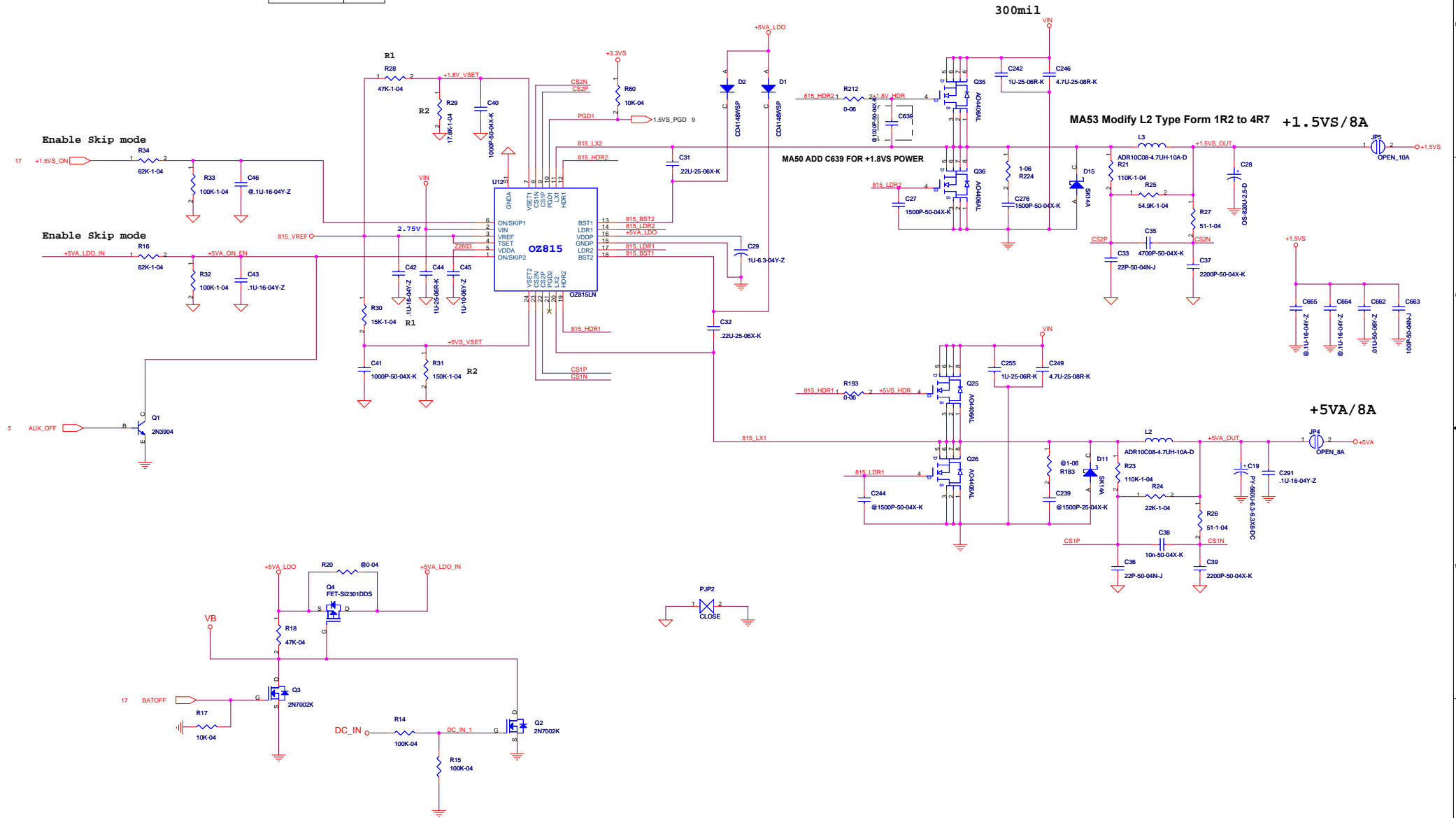
VID TABLE

	6	5	4	3	2	1	0	Vcore	Status
0	0	0	1	0	0	0	1	1.2875	(HFM)
0	0	0	1	1	0	0	0	1.2000	Boot Vout
0	0	0	1	1	1	0	0	1.1500	Merom(HFM)
0	0	1	1	0	1	0	1	0.8375	Y&M(LFM)
0	0	1	1	1	0	1	1	0.7625	Y&M(Deeper Sleep)
1	1	1	1	1	1	1	1	0.0000	Shut down

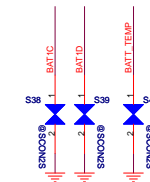


+1.8V/+5V_ON Voltage	Mode
<0.4V	OFF
>0.6V	PWM
>2.1V	SKIP

$$\text{Output Voltage} = [V_{\text{ref}} \times R2 / (R1 + R2)] \times 2$$



# CHARGER

$$V_{chg} = RAD1 \cdot I_{rsense} \cdot 10$$


Pin 6 connection diagram for the CN6 connector. The connector has pins labeled H1, 1, 2, 3, 4, 5, 6, and H2. Pin 6 is connected to CON\_BAT\_M7\_C144BN-107A8-L\_ATP.

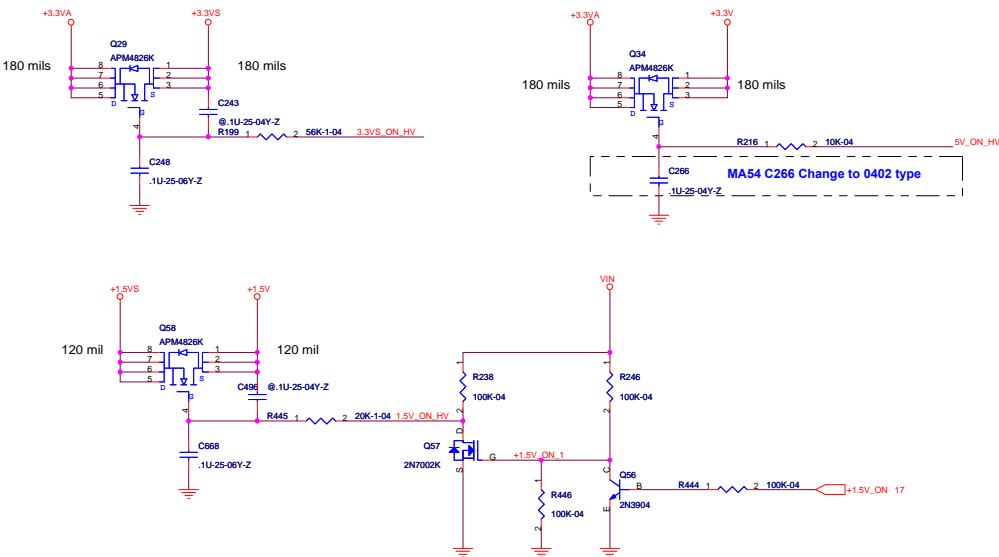
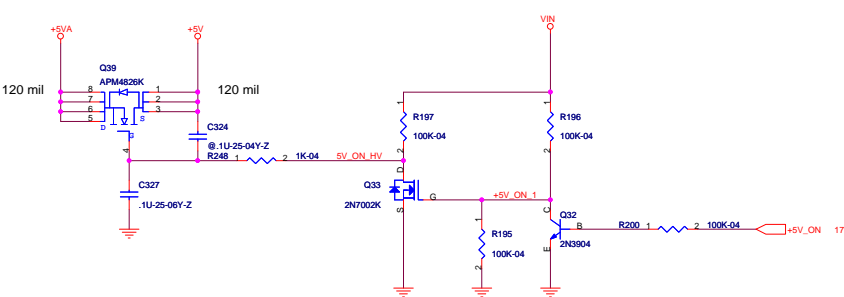
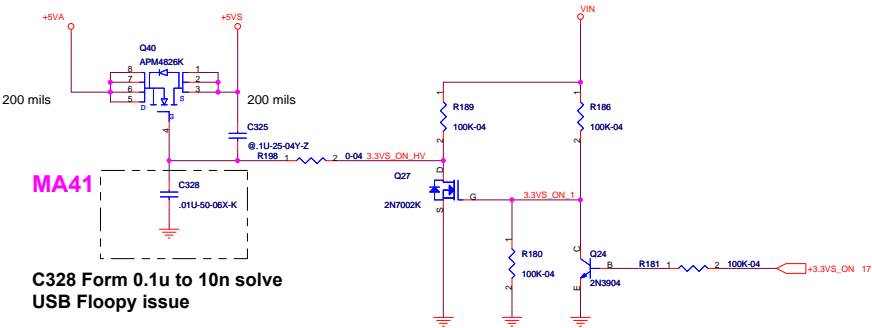
**MA36**  
CHANGE BATT PIN2  
GND Form Battery to DGND

17.6V->BAT\_V=2.2V  
 16.8V->BAT\_V=2.1V  
 13.2V->BAT\_V=1.65V  
 12.6V->BAT\_V=1.575V  
 9.0V->BAT\_V=1.125V

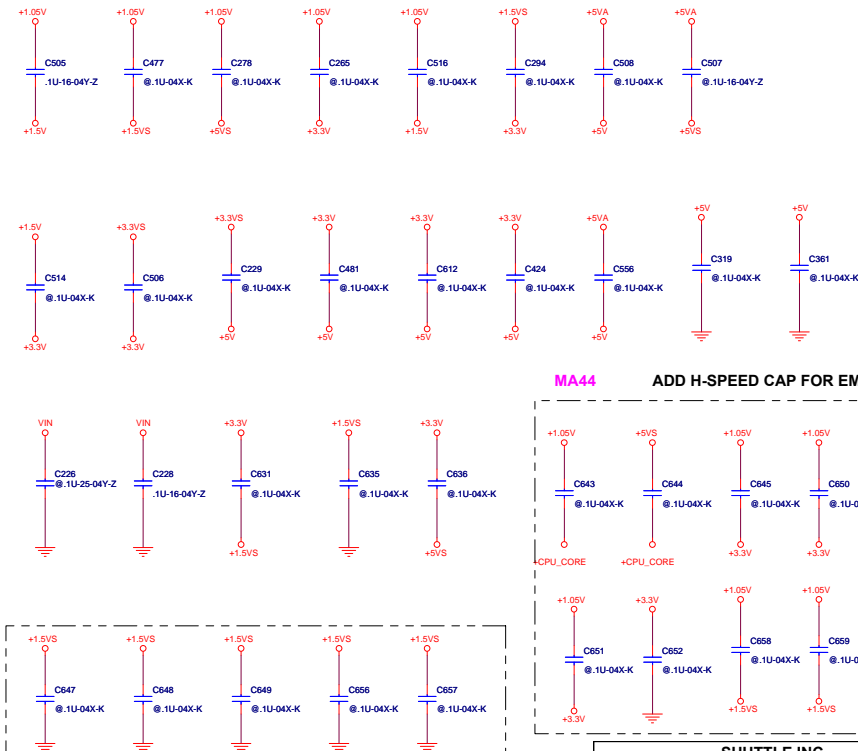
**Charge / Discharge Detect**

The schematic shows a charge/discharge detection circuit. A voltage divider consisting of R48 (20K-1-04) and R53 (1.5K-1-04) is connected to the CHG\_REF pin. The divider is biased by VIN through R49 (16.5K-1-04). The op-amp (U11A, GS358SF) is configured with a feedback network of R49 and R54 (1.5K-1-04). The op-amp output is connected to the BAT\_I pin. The circuit is powered by VIN and GND. A capacitor C62 (1U-6.3-04Y-Z) is connected to the CHG\_REF pin. A diode D10 (M-SOD323, UDZSNPTE-173.3B) is connected to the BAT\_I pin. A capacitor C224 (0.1U-16-04Y-Z) is connected to the BAT\_I pin. The op-amp is also connected to GND through R58 (0.06) and R59 (1.5K-1-04). The op-amp is powered by VIN through C221 (1000P-50-04X-K) and C222 (0.1U-25-06Y-Z).

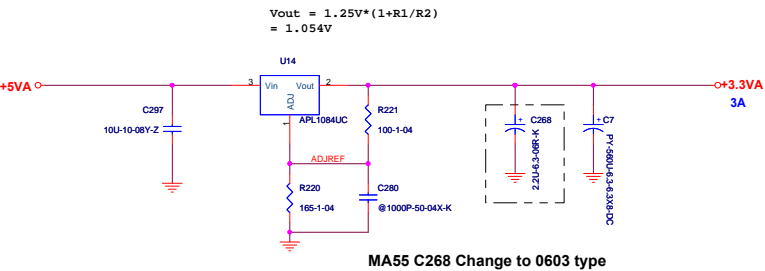
VCCSW



HIGH-SPEED CAP



LDO



RA to RB Modify list:

Symbol	Modify Item	Recheck layout and BOM	Page	Note
M61	ESM change power plane from 13.0 to VDDSE Sense 00M value by AUX_OFF issue P025	Layout NOT READY		
M62	CHG 12.0V Sense 00M to 13.0V sense 00M P250 P025	Layout NOT READY		
M63	NOV 00M AND 00M121 P025 P025	Layout Modify OK		
M64	NOV 00M AND 00M121 P025 P025	Layout Modify OK		
M65	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M66	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M67	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M68	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M69	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M70	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M71	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M72	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M73	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M74	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M75	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M76	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M77	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M78	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M79	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M80	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M81	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M82	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M83	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M84	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M85	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M86	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M87	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M88	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M89	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M90	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M91	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M92	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M93	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M94	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M95	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M96	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M97	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M98	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M99	NOV 00M AND 00M121 P025 P025	Layout NOT READY		
M100	NOV 00M AND 00M121 P025 P025	Layout NOT READY		